Single Synchronous Buck Pulse-Width Modulation (PWM) Controller

The ISL6406 is an adjustable frequency, synchronous buck switching regulator optimized for generating lower voltages for the distributed DC/DC architectures. The ISL6406 offers an adjustable output voltage.

Designed to drive N-Channel MOSFETs in synchronous buck topology, the ISL6406 integrates the control, output adjustment and protection functions into a single package.

The ISL6406 provides simple, single feedback loop, voltage-mode control with fast transient response. The output voltage can be precisely regulated to as low as 0.8V. The error amplifier features a 15MHz gain-bandwidth product and 6V/µs slew rate which enables high converter bandwidth for fast transient performance.

Protection from overcurrent conditions is provided by monitoring the $r_{DS(ON)}$ of the upper MOSFET to inhibit PWM operation appropriately. This approach simplifies the implementation and improves efficiency by eliminating the need for a current sense resistor.

The wide programmable switching frequency range of 100kHz to 700kHz allows the use of small surface mount inductors and capacitors. The device also provides external frequency synchronization making it an ideal choice for DC/DC converter applications.

Features

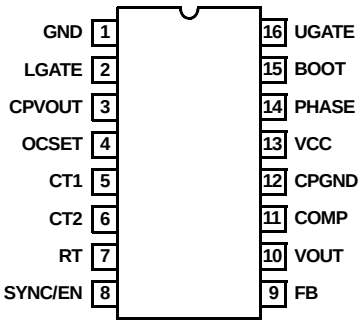
- Operates from 3.3V/5V Input
- 0.8V to V_{IN} Output Range
  - 0.8V Internal Reference
  - ±1.5% Reference Accuracy
- Simple Single-Loop Control Design
  - Voltage-Mode PWM Control
- Fast Transient Response
  - High-Bandwidth Error Amplifier
- Lossless, Programmable Overcurrent Protection
  - Uses Upper MOSFET's $r_{DS(on)}$
- Programmable Switching Frequency 100kHz to 700kHz
- External Frequency Synchronization
- Two Device Options Available
  - ISL6406 . . . . . Adjustable Output Voltage
- Internal Soft-Start
- QFN Package Option
  - QFN Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Product Outline
  - QFN Near Chip Scale Package Footprint; Improves PCB Efficiency, Thinner in Profile
- Pb-Free Plus Anneal Available (RoHS Compliant)
  - Designated with "Z" Suffix (Refer to Note)

Applications

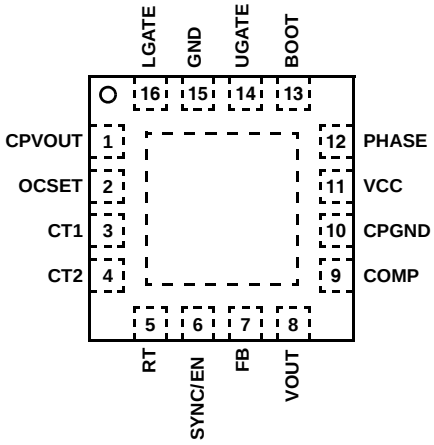
- 3V/5V DC/DC Converter Modules
- Distributed DC/DC 3.3V, 2.5V and 1.8V Power Architectures for DSP, Logic, and Memory
- Power Supplies for Microprocessors
  - PCs
  - Embedded Controllers
- Memory Supplies
- Personal Computer Peripherals

Pinouts

ISL6406,
(16 LD SOIC/TSSOP)
TOP VIEW



ISL6406,
(16 LD QFN)
TOP VIEW



Ordering Information

PART NUMBER*	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6406IB	ISL6406IB	-40 to +85	16 Ld SOIC	M16.15
ISL6406IBZ (See Note)	6406IBZ	-40 to +85	16 Ld SOIC (Pb-free)	M16.15
ISL6406IR	ISL 6406IR	-40 to +85	16 Ld 5x5 QFN	L16.5x5B
ISL6406IRZ (See Note)	ISL6406 IRZ	-40 to +85	16 Ld 5x5 QFN (Pb-free)	L16.5x5B
ISL6406IV	ISL64 06IV	-40 to +85	16 Ld TSSOP	M16.173
ISL6406IVZ (See Note)	6406 IVZ	-40 to +85	16 Ld TSSOP (Pb-free)	M16.173

*Add “-T” suffix to part number for tape and reel packaging.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

Supply Voltage, VCC (Note 1) . . . . . +7.0V
Absolute Boot Voltage, V_{BOOT} . . . . . +15.0V
Upper Driver Supply Voltage, V_{BOOT} - V_{PHASE} . . . . . +6.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to VCC +0.3V
ESD Classification . . . . . Class 2

Operating Conditions

Temperature Range
ISL6406 . . . . . 0°C to +70°C
ISL6406 . . . . . -40°C to +85°C
Supply Voltage Range . . . . . 3.3V ±10%

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SOIC (Note 2)	70	N/A
TSSOP (Note 2)	90	N/A
QFN (Notes 3, 4)	35	4.5

Maximum Junction Temperature (Plastic Package) . -55°C to +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Please refer to the Typical Application Schematics (page 3) for 3.3V/5V input configuration.
2. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
3. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
4. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended operating conditions unless otherwise noted. Refer to Block Diagram and Typical Application Schematic. V_{CC} = +3.3V. Typical values are at T_A = +25°C.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} SUPPLY					
Shutdown Supply Current	SYNC/EN = GND	-	20	50	µA
Operating Supply Current (Note 5)	RT = 64.9kΩ	7	9.8	11.5	mA
REFERENCE VOLTAGE					
Nominal Reference Voltage		-	0.8	-	V
Reference Voltage Tolerance		-1.5	-	1.5	%
	T_A = 0°C to +70°C	-1.8	-	1.8	%
	T_A = -40°C to +85°C	-2.1	-	2.1	%
ERROR AMPLIFIER					
Open Loop Voltage Gain (Note 6)		-	82	-	dB
Gain-Bandwidth Product (Note 6)		14	-	-	MHz
Slew Rate (Note 5)	COMP = 10pF	4.65	6.0	9.2	V/µs
CHARGE PUMP					
Nominal Charge Pump Output	V_{CC} = 3.3V, No Load	4.8	5.1	5.5	V
Charge Pump Output Regulation		-5.0	-	5.0	%
POWER-ON RESET					
Rising CPVOUT POR Threshold	T_A = 0°C to +70°C	4.20	4.35	4.5	V
	T_A = -40°C to +85°C	4.1	4.35	4.6	V
CPVOUT POR Threshold Hysteresis		0.3	0.5	0.9	V
OSCILLATOR					
Gate Output Frequency Range	RT = 200kΩ	80	100	120	kHz
	RT = 64.9kΩ	250	300	340	kHz
	RT = 26.1kΩ	650	715	770	kHz
Sawtooth Amplitude	Peak-to-Peak ΔV_{OSC}	1.1	1.4	1.7	V

Electrical Specifications Recommended operating conditions unless otherwise noted. Refer to Block Diagram and Typical Application Schematic. V_{CC} = +3.3V. Typical values are at T_A = +25°C. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Sync. Frequency Range (Note 6)	1.1 Times the natural switching frequency.	110	-	770	kHz
Minimum Sync Pulse Width (Note 6)		-	40	100	ns
PWM Maximum Duty Cycle		-	96	-	%
GATE DRIVER OUTPUT (Note 6)					
Upper Gate Source Current	V_{BOOT} - V_{PHASE} = 5V, V_{UGATE} = 4V	-	-1	-	A
Upper Gate Sink Current		-	1	-	A
Lower Gate Source Current	V_{VCC} = 3.3V, V_{LGATE} = 4V	-	-1	-	A
Lower Gate Sink Current		-	2	-	A
SOFT-START					
Soft-Start Slew Rate	f = 300kHz, T_A = 0°C to +70°C	6.2	6.7	7.3	ms
	f = 300kHz, T_A = -40°C to +85°C	6.2	6.7	7.6	ms
	Internal Digital Circuit Clock Count (Soft-start time varies with frequency)	-	2048	-	Clk Cycles
OVERCURRENT					
OCSET Current Source	T_A = 0°C to +70°C	18	20	22	µA
	T_A = -40°C to +85°C	16	20	23	µA

NOTES:

5. This is the V_{CC} current consumed when the device is active but not switching.
6. Guaranteed by design.

Typical Performance Curve

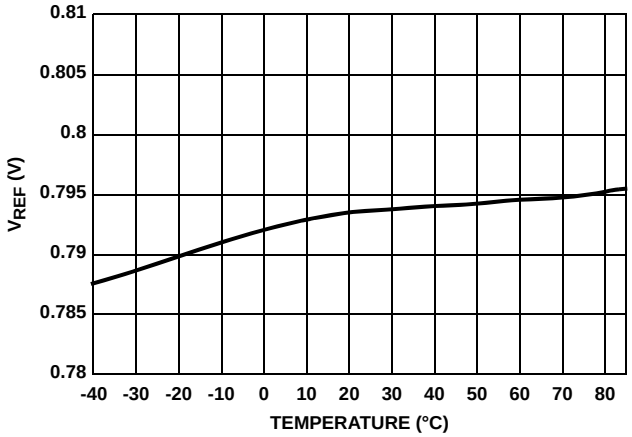
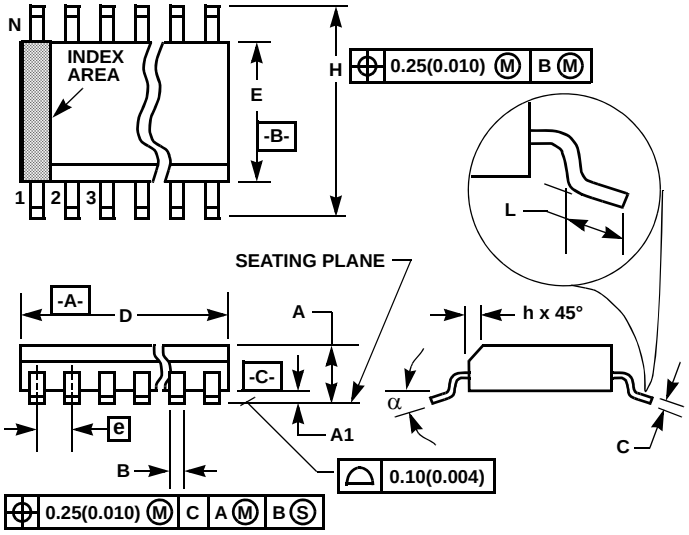


FIGURE 1. REFERENCE VOLTAGE vs TEMPERATURE

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-